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This report presents results of using a commercial 2.5G 12x14 MAC filter chip to accomplish interpolation for radar signal processing. The report also develops a next generation architecture that results in a 500 MSPS digital interpolator and tap delay line. This will allow the replacement of a large quantity of analog signal processing equipment; improving signal quality and channel matching, while reducing costs by $2-4M per system. The interpolator will accept inputs at 10 MSPS complex, provides a fine frequency shift (0.1Hz, 100dBc), and interpolates the signal up to 320 MSPS (spec), 480 MSPS (goal). A second chip (TAP) is defined that accepts the interpolated clutter return and seeker pulse, delays it 1-128 samples, multiplies them, and adds the result to other tap delay points. The TAP chip may alternatively frequency shift the interpolated signal in 6 MHz steps (90 dBc). The two chips can be used together to build a cable TV head-end by using two chips per 5 MBaud, 64 QAM input.

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1.0 Introduction

This is the final report for SBIR topic A94-048. It is divided into two sections reflecting the two major tasks performed. Section two presents trades and work performed that resulted in using the GC2011 to build an improved digital quadrature modulator (DQM). Section three presents a selected architecture for an advanced DQM that was proposed for phase two. This would result in large scale replacement of analog IF equipment with digital counterparts.

2.0 Improved DQM

The phase I objectives were to do design work to provide higher data rate, with a flatter response and better stop bands than current system. A comparison between the existing system, phase I objectives and accomplishments, and phase II objectives as shown in table 1.

Table 1: Comparison of Existing to Phase I Objectives

	Existing	Phase I Objectives	Phase I Accomplish ment	Phase II Objectives
Maximum Input BW	800 kHz	Not stated	3.75 MHz	7.5 MHz
Passband Ripple	0.6 dB	Not stated	<0.15 dB	0.1 dB
Stopband	65 dB	65 dB	80 dB	85 dB
Fcenter	6 MHz	40 MHz	20 MHz	120 MHz
Fsample	24 MSPS	160 MHz	80 MSPS	480 MSPS

Several candidate architectures using the existing GC2011 chips were examined. These provided stop bands from 70 to 150 dB, and had maximum output sample rates from 80 to 320 MSPS. The number of chips required to implement the filters varied from 2 to 6, with a corresponding variation in recurring costs. Figure 1 shows the block diagram of the best performance architecture.

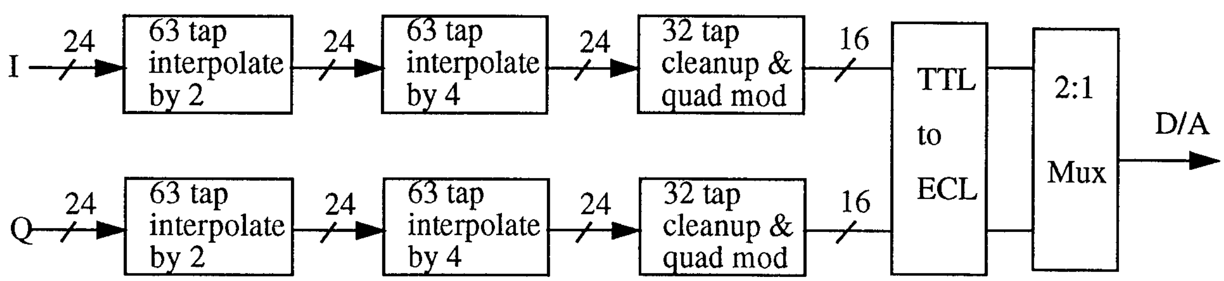

Figure 1. 150 dB Interpolate by 16 Architecture

Figure 2 shows the resulting spectral performance with a general stopband of nearly 150 dB and a single lobe at 100 dB suppression. This configuration requires 6 GC2011's per channel.

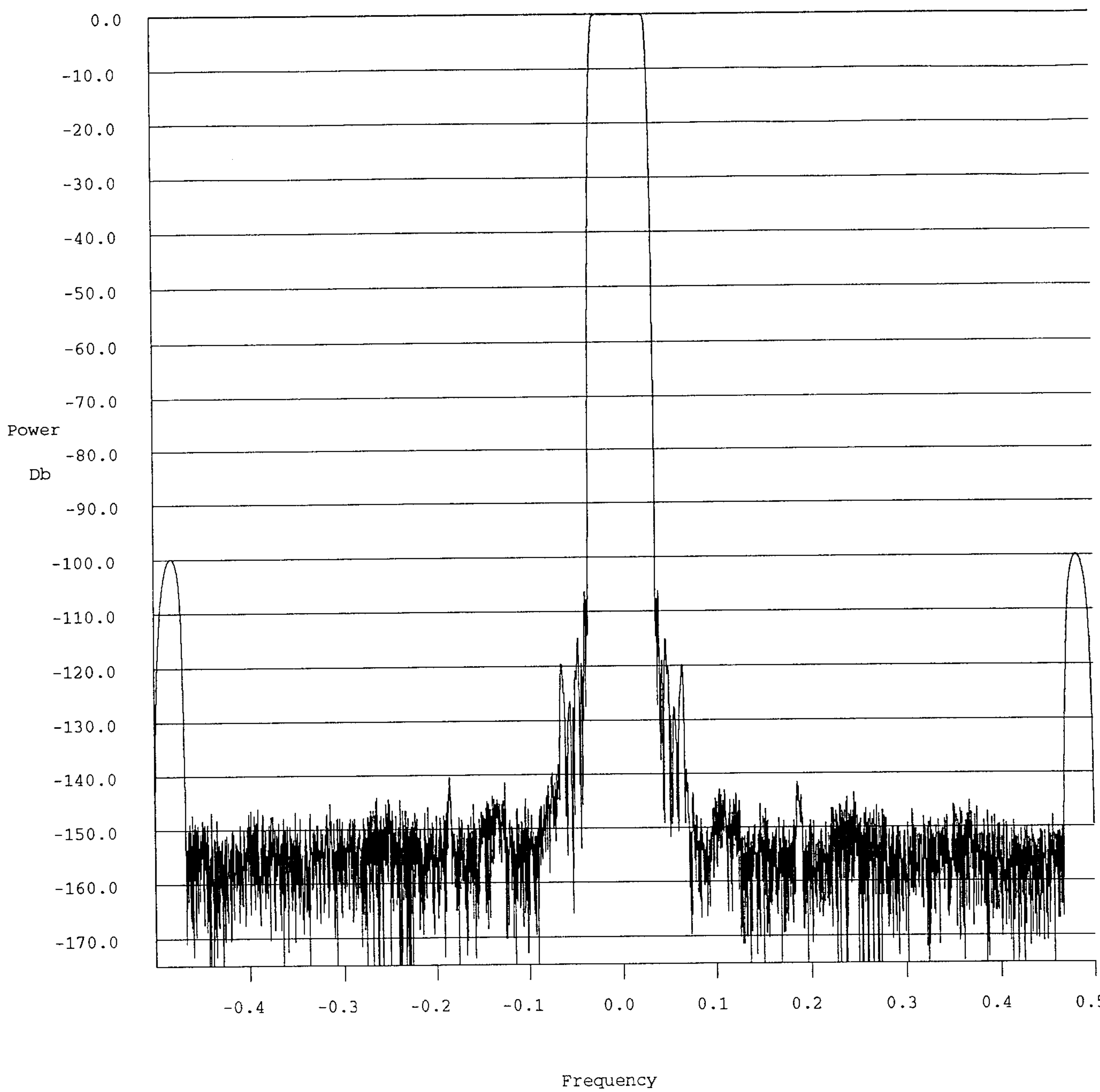

Figure 2. Overall Spectral Response for 6 Chip Interpolator

The customer then decided that 80 dB stop band was sufficient given the state of the art in D/A's and the likely near term improvements. The resulting configuration is shown in figure 3.

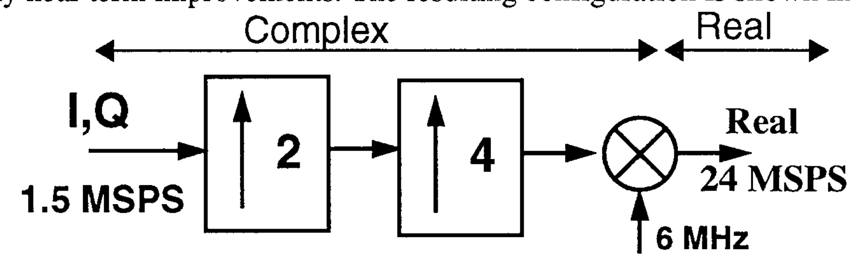

Figure 3. Phase I Resulting Architecture

This provides significantly greater performance than the D/A can support allowing the system to take advantage of future improvements in D/A technology w/o having to rework the digital section. Several other candidates were considered along the way offering performance and cost between these two. The customer ran tests on a variety of D/A before deciding on an approach.

3.0 Advanced DQM

Hardware in the loop radar simulation requires signal models generated in computers to be translated up in frequency, shifted to simulate doppler effects, time delayed to mimic range delays, multiplied by the radar pulse to generate a simulated radar return. For clutter modelling many (typically 16) different range delays are required to simulate the return from the local terrain. A Digital Quadrature Modulation (DQM) is used to take computer generated baseband (complex) returns, substantially interpolate them up in sample rate, then convert to real and perform an Fs/4 frequency shift. Historically, the signal is then converted into the analog domain. Once in the analog domain the signal is mixed up in frequency, and shifted in frequency to mimic doppler. The radar pulse is delayed, then enters a 16 element analog tap delay line. Each of 16 different delays are multiplied by a DQM output and then all 16 are summed together. The current system consumes three racks per RF channel at a cost of more than a million dollars for the WDQM, doppler shifting, and tap delay line.

During the phase I effort architectural studies were performed and it was found that a second generation DQM could be built that would make the entire tap delay line, DQM path, doppler shifting, multiplying, and summing digital. This would provide many advantages in eliminating many imperfections of the analog tap delay line (triple travel, non-linearities, calibration requirements) as well as substantially reducing the size and cost. A complete RF channel with 16 taps each for horizontal and vertical polarization would fit onto 5 cards (4 for digital processing and 1 for a pair of D/A's) at a cost of less than $120k.

Similar results are expected in the digital cable TV headend market where many TV channels will be combined into one MPEG stream at 5 MSPS. Many MPEG streams will then be combined onto a cable. Combining them digitally will allow perfect frequency spacing, amplitude control, and I/Q balance. Outputting the results at a high sample rate with many MPEG streams will greatly reduce the amount of mixing and filtering required to build up a full cable signal stream. A chip set that can be assembled to build a full cable signal stream should help achieve significant cost, and maintenance savings. Already the technique of digitally interpolating a signal stream to high sample rates is being used for direct broadcast satellite TV where a 30 Mbaud QPSK signal is digitally interpolated up to 250 MSPS prior to conversion to analog. This is done to reduce phase noise in the transmitted signal. The next generation uplink system is expected to go to 500 MSPS.

Several alternative second generation architectures were examined. These provided the significant benefit of allowing the digitalization of the tap delay line, doppler shifting, and summing network, as well as eliminating a large number of analog mixers. A substantial volume of analog hardware is replaced by a single card of digital hardware that requires no calibration. This also allows extension to greater number of taps - something desired but not feasible with analog equipment due to the accumulated effects of various imperfections. Two chips were defined as part of the architecture studies, a DQM chip and a TAP chip. Figure 4 shows the resulting system block diagram for one RF channel.

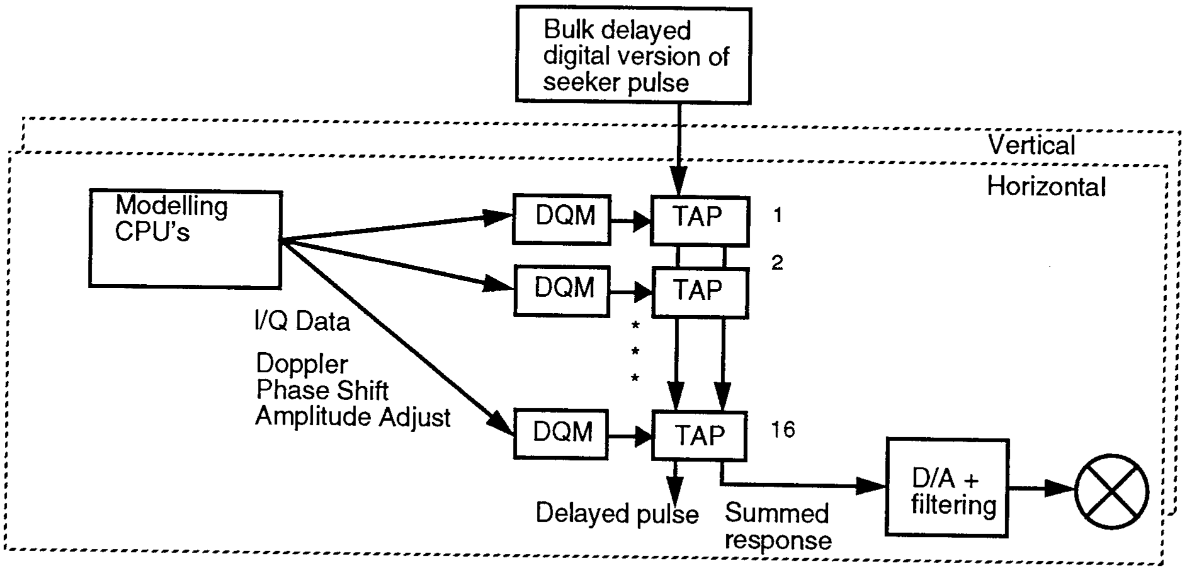

Figure 4. System Block Diagram for One RF Channel

Figure 5 shows the DQM chip. A small amount of flexibility is included so it can serve several purposes. The requirements for the DQM chip are to provide interpolation by 48, with >85dB stop bands, <0.1dB ripple across a 75% input passband, all spurs should be <-90dBc. A frequency shift of up to 5 MHz, with a resolution of at least 0.1Hz is required. For some applications, gain and phase are the inputs rather than I and Q. When used with a digital tap delay line the output should be complex, centered near DC. When used with an analog tap delay line the output should be real, centered at Fs/4. For near term applications the chip must also support input at 1.5 MSPS, and output real data at 48 MSPS centered at 12 MHz. Additional requirements to support commercial application is that the chip should support 5 MSPS filtering with a raised root cosine for QAM modulation. The required maximum output frequency (Fmax) is 320 MHz, the goal is 480 MHz.

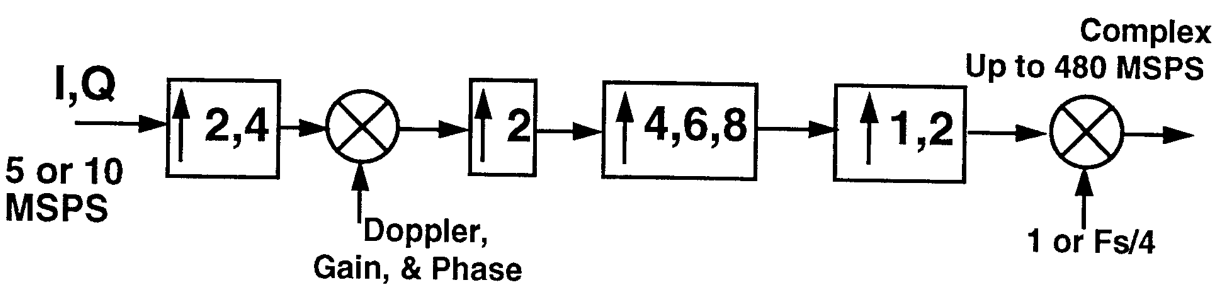

Figure 5. Digital Quadrature Modulator Chip Block Diagram

The requirements for the TAP chip are to provide delay of 24 bit complex (12 bits I, 12 bits Q) seeker samples at Fmax. The delay needs to be an effective 1-128 samples. The chip must also accept 28 bit complex (14 bits I, 14 bits Q) from a DQM chip. These two must be multiplied, and frequency shifted by Fs/4, retaining only the real part. Finally, the result must be added to a sum tree to allow multiple paths to be added together (up to 32 paths). The final TAP chip in the chain must support rounding at 12,14, or 16 bits to optimize performance of the D/A. The required Fmax is 320 MHz, the goal is 480 MHz. Support for commercial cable TV modulation applications requires the addition of a frequency shift with 6 MHz resolution, >90 dB SFDR. An NCO can feed the first complex multiplier (instead of the seeker pulse) to satisfy this requirement. Figure 6 shows the TAP.

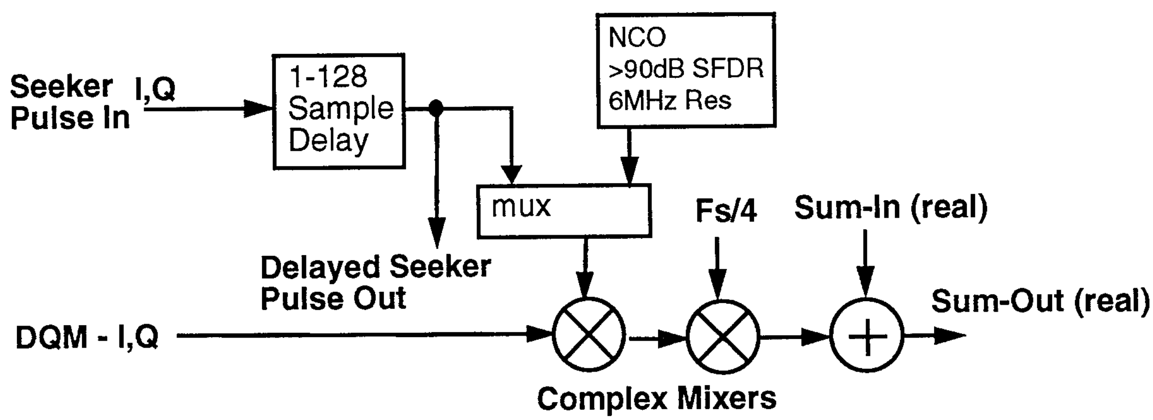

Figure 6. TAP Delay Line Chip Block Diagram

3.1 DQM Detailed Description

The section will describe in detail each block w/in the proposed DQM chip.

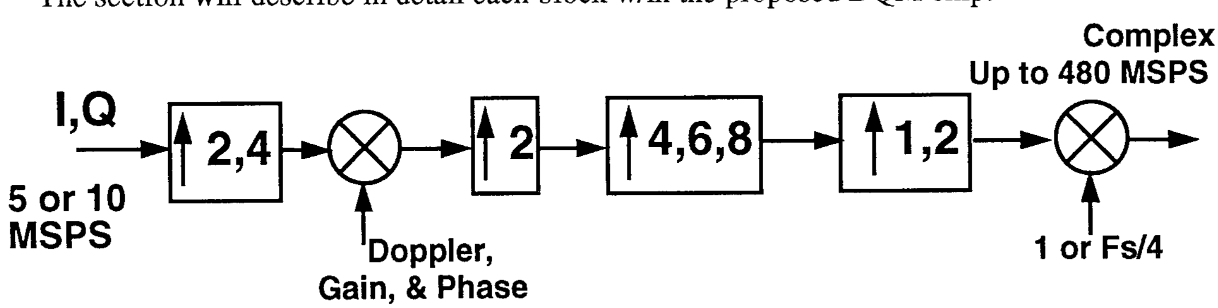

Figure 7. Digital Quadrature Modulator Chip Block Diagram

The first block is an interpolate by 2 or 4 with programmable coefficients. When the block is interpolating by 2 input data is accepted at rates up to 10 MSPS complex. The interpolator is built using a FIR structure with the internal logic operating at 8 times the input rate. This allows reuse of the computing hardware and significantly reduces the total hardware required. The filter structure takes advantage of the symmetry by using a preadder, as well as the interpolation by two by rotating coefficients rather than multiplying by zero data. The filter cell is very similar to the one used in the GC2011 chip, simplified since there are fewer modes to operate in. The number of taps will be determined during the preliminary design phase. Initial estimates are that 33 taps is barely adequate. We have used 63 taps in previous chips to allow for more stringent future requirements. The chip sizing in the proposal assumes 63 taps. The design effort (hence the NRE price) is unaffected by the number of taps. The power will be impacted by the number of taps. Since power is one reason for partitioning the design into two chips this will be reevaluated at PDR. 15 bit data and 16 bit coefficients are planned.

The first block may also be used in an interpolate by 4 mode. This is accomplished by simply inserting a zero between samples. When interpolating by 4 one cannot take advantage of both the filter symmetry and the fact that 3/4 of the input data are zeros because the non-zero data does not line up onto the same coefficients. This can be seen in the GC2011 data sheet in that the interpolate by 2 and interpolate by 4 filter lengths are identical. Inserting a zero between samples allows us to achieve optimum usage of the hardware since we will still get all the optimizations available in an interpolate by two mode. When using the chip for a QAM modulator (cable TV applications) the first filter must interpolate by 4 to allow room for the required excess bandwidth. A root raised cosine filter is required with a typical excess bandwidth of 20 to 30%. Approximately 150,000 transistors are required for this block.

The next block performs a frequency shift. An internal NCO is planned that will reuse the NCO from a chip currently under development. This NCO provides greater than 100 dB SFDR. The frequency resolution needs to be increased from 0.4 Hz to 0.1 Hz. To achieve the desired frequency resolution and the SFDR, a combination of lookup table and computation is done. A straight lookup table would be too large.

The third block interpolates by two again. This is the same as the first block except the input rate is doubled and the number of coefficients is halved. The same amount of hardware is required as for the first block. To minimize NRE the first design will be reused as much as possible, so the coefficients will be programmable. This filter must interpolate by two AND provide pre-emphasis to compensate for the droop in the subsequent CIC filter. A set of coefficients suitable for use in this application will be provided.

The fourth block is a CIC interpolation filter[1]. This device operates at up to 40 MHz at the input and interpolates up by 4,6, or 8. CIC filters are particularly efficient at interpolating or decimating signals by variable amounts if the desired total interpolation/decimation is at least 8 (CIC interpolation by 2). They are widely used in Graychip products. The output of this filter operates at speeds up to 240 MHz. At these speeds a different design style is required since the normal design style is used for speeds up to 100 MHz. A high speed logic design style known as TSPC[2] is used. This design style has been used by others to build NCO's, error correction chips, and serial communication chips. Graychip has used this design style for chips operating at speeds

1. Hogenhaugher, Eugene V., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech and Signal Processing, April 1981.
2. Yuan, Jiren and Svensson, Christer. High-Speed CMOS Circuit Technique, IEEE Journal of Solid-State Circuits, February 1989

up to 1GHz. Almost all of the high speed blocks required for the DQM and TAP chips have similar blocks in the GC1016. Specifically, the GC1016 has a 5 stage 40 bit CIC decimation filter. The DQM requires a 4 stage 32 bit CIC interpolation filter. These will use the same 4 bit slices.

The fifth block is an optional interpolate by two filter. Since the pass band is very close to DC and the image (if interpolating) is very close to Fs/2 there is a wide transition range. A simple filter will suffice (taps of 1,4,6,4,1). The logic operates at 240 MHz so two output points will be computed in parallel. A total of 4 adders are required to build this very simple filter.

Finally, an optional Fs/4 frequency shift is applied to allow real outputs of the DQM. This will allow the chip to be used in systems for which a digital tap delay line is unavailable or undesirable. The Fs/4 shift is particularly simple consisting of multiplexing between the I and Q channels and multiplying by +/- 1. For digital tap delay operations the Fs/4 shift is not desired so it must also support a simple multiply by 1 all the time.

Clocking and input/output are challenging when operating at 500 MHz. We have build chips that accept data at 500 MHz before. We have also had chips drive their outputs at over 1000

MHz before. The figure below shows the eye diagram of the GC5003 chip operating at 500 MHz showing clean edges and 500 pS rise and fall times.

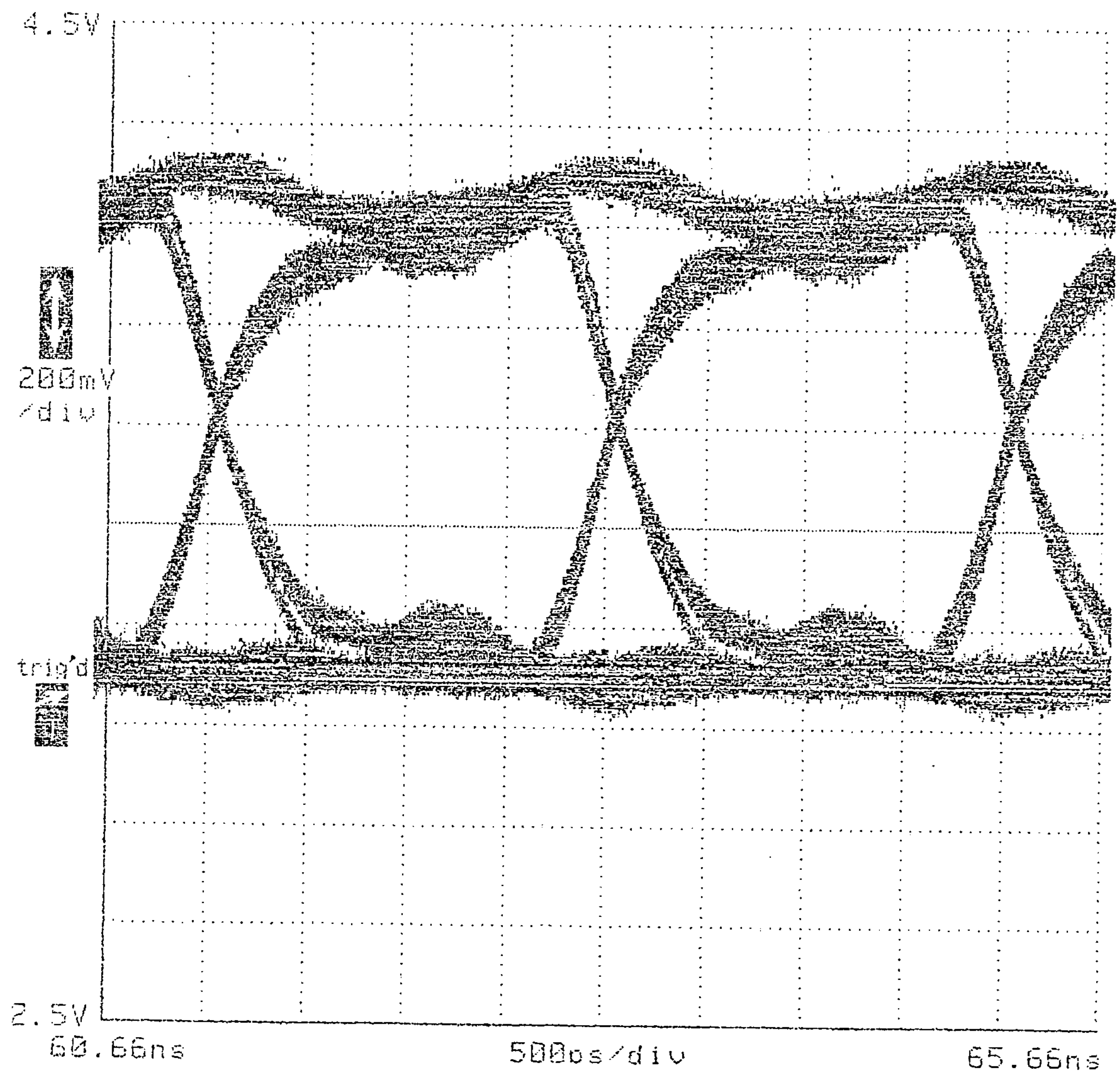

Figure 8. GC5003 Eye Diagram at 500 MHz

Previous high speed chips such as the GC5003 provided an output clock synchronous with the data output. The new challenge with the DQM chip is that the output must be synchronous with the board, which is difficult to do at 480 MHz due to the clock buffer delays within the chip. The output data must be synchronous to the board clock because the system design requires the TAP chips to accept data both from the DQM chip and from the previous TAP chip. The previous designs resulted in a significant delay on the internal clock and hence would create an excessive clock to output delay if the board clock were used to sample the chip's output. A more sophisticated technique is required here This may be done in one of two ways.

An internal delay lock loop can be used to drive the internal clock to be phase synchronous with the external one. Such circuitry entails sufficient risk that risk reduction measures are appropriate. A test chip will be fabricated using MOSIS facilities in an HP 0.5 micron process to test the clock generator as well as the ECL I/O. This is the baseline plan.

An alternative technique would be to have each TAP chip accept three clocks. In addition to the board clock the TAP would accept input clocks from the DQM and previous TAP chip (sum-in). These would be used to latch the inputs. Transferring the data to the internal clock would then be done at a fanned out 240 MHz where there is more timing margins.

The total transistor count for this chip is 350,000 transistors. The power is estimated at 3 Watts. The pin count is estimated at 140 to 200 pins depending on whether single-ended or differential I/O is used.

3.2 TAP Detailed Description

This section will discuss the TAP chip block by block. The TAP chip block diagram is repeated below for convenience.

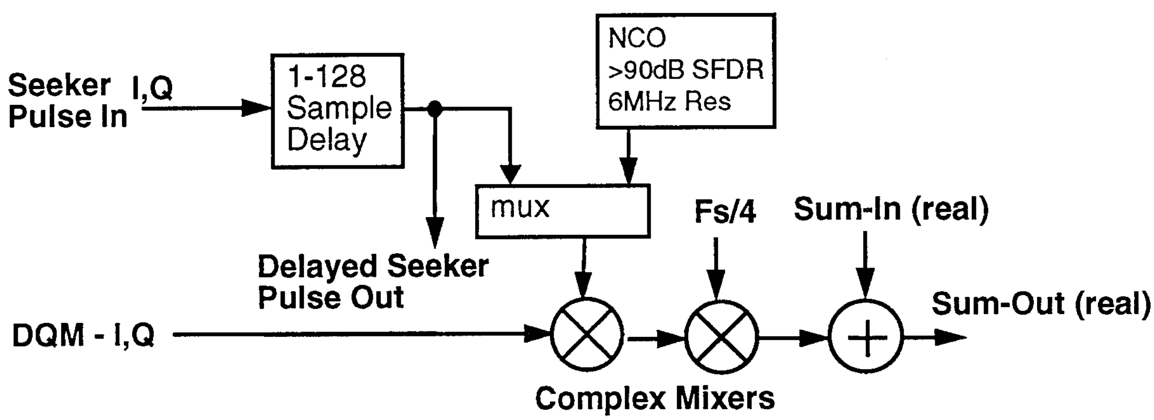

Figure 9. TAP Delay Line Chip Block Diagram

The first block is a 1 to 128 sample delay, operating at up to 480 MHz (goal 320 MHz spec), on 12 bit I and Q samples. This block is implemented by using high speed logic to build a 1:6 fanout, driving a wide word memory for the bulk of the delay, feeding a 6:1 fan-in, and a variable delay of 1 to 6 cycles. In addition to the variable delay of 1 to 128 samples there will be a fixed delay of a few samples due to pipeline delays. This can be corrected for by providing matching delays on the sum-in to sum-out and sync-in to sync-out paths and decreasing the delay in the bulk memory (DRFM). The wide word (6*24 or 144 bit), shallow (22 words deep) memory operates at 80 MHz with simultaneous read and write. This is similar to requirements for other memory systems we have built. Graychip routinely builds internal memories operating at speeds up to 100 MHz.

The first complex mixer multiplies the seeker pulse by the DQM output. It is simply a complex multiplier very similar to one contained within the GC1016. Zero bias rounding is used to prevent any spurs at DC. Only the real portion of the multiply needs to be computed so two real multiplies are required. Since the data is operating at twice the speed of the logic four physical multipliers are used. A similar scheme is used in the GC1016. These four multipliers represent a lot of high speed logic but since it is so similar to previous work we have done it does not entail substantial risk

The Fs/4 mix again is simply multiplexers and a multiply by +/- 1. Very little logic is used here.

Finally, the sum path allows the various DQM/TAP results to be combined into a single data-stream. High speed operation is achieved by heavily pipeling the adder. Bits are skewed (higher order bits arrive clock cycles later than lower order bits) to allow latches to be placed into the carry chain for maximum frequency operation. The sums are passed from one TAP chip to the next still skewed to minimize latency. An optional deskew function is incorporated that is only used in the final TAP chip to deskew the sum prior to applying it to the D/A. The final chip must also round the result to match the capability of the D/A. Programmable rounding points of 12,14, and 16 bits are planned.

The chip is estimated at 150,000 transistors, using 2 Watts, and requires from 200 to 300 pins depending on whether single-ended or differential signalling is used for the high speed I/O.

3.3 Commercial Applications

The primary commercial application for this is digital cable TV. Here each MPEG stream must be modulated into a 5 MBaud, 64 QAM signal. Several such signals must then be FDM multiplexed into a single composite bandwidth for transmission down the coax cable plant. The DQM chip performs the modulation function and interpolates the signal to a high sample rate. The TAP chip is then used to frequency translate the signal and sum many such signals together to form a single output stream. The resulting data stream is then converted to analog prior to transmission down the cable as shown in the following figure.

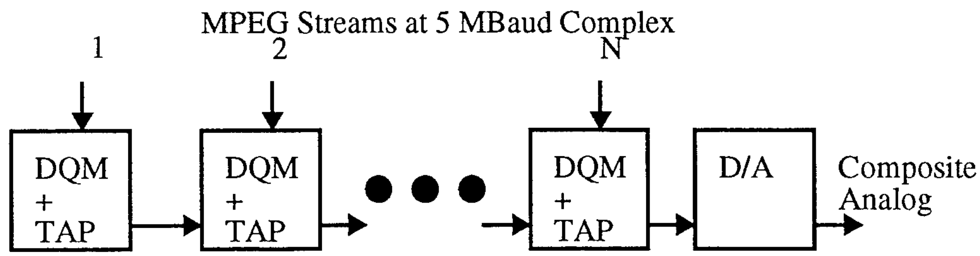

Figure 10. Digital Cable TV Modulation and Multiplexing

Not only will this provide a significant signal quality improvement, it should also be less expensive. Other commercial applications include modulation for point to point private microwave transmission such as done by Digital Microwave Corporation.

The primary government use for such a chip set is the advanced radar environment simulator where it will save sufficient money to pay for the development several times over with every RF channel built.

This chip is planned to be used by MICOM in their next generation advanced radar environment simulator. The existing GC2011 has already found use in two government systems in just two months. As additional applications are identified they may need the enhancements being provided by this program - or may provide additional funding to incorporate enhancements desired by this program.

Private sector applications for the chip are currently in the exploratory stage. One US based commercial telecommunications digital radio supplier is examining the chip for use in their next generation radios to compete in the international marketplace. The chip is also being considered for use in prototype HDTV receivers. (It is too large for use in production models but its flexibility provides an excellent test bed for evaluating the performance impact of various hardware saving measures like number of bits in the data or coefficients, number of taps, etc.).

Graychip is already in the business of providing sophisticated signal processing chips to both the government and commercial markets. We have begun discussions for marketing our product line internationally. While the specific enhancements required to support MICOM may not have direct commercial application the general purpose filtering chip does and either can be customized to provide just those features required for a commercial application at minimum production costs.